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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/758,586	01/15/2004	David Arnold Luick	ROC920030258US1	5898

7590 07/25/2006

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EXAMINER	
PUENTE, EMERSON C	

ART UNIT	PAPER NUMBER
2113	

DATE MAILED: 07/25/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/758,586	LUICK, DAVID ARNOLD	
	Examiner	Art Unit	
	Emerson C. Puente	2113	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 January 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6,9,11-16,19 and 20* is/are rejected.

7)☒ Claim(s) *7,8,10,17 and 18* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *15 January 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This action is made **Non-Final.**

Claims 1-20 have been examined.

Claim Objections

Claims 10 and 15 are objected to because of the following informalities:

In regards to claim 10 and 15, the limitation "a history"(see line 3 of claim) is not storage, and as such is unable to store/save information. Please change "means for saving status of the function disable register and the error in a history after the error is reproduced" to "means for saving status of the function disable register and the error in a history **table** after the error is reproduced".

Appropriate correction is required.

Claim Rejections - 35 USC § 101

35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

Claims 11-15 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter.

In regards to claim 11-15, the claimed "signal-bearing medium" as described in the specification page(s) 11, lines 3-5, includes, among other examples, communications medium,

such as a computer or telephone network, e.g., the network, which is nonstatutory. As such, the claim is not limited to statutory subject matter and is therefore non-statutory.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1,2,5,6,9,11, and 14 are rejected under 35 U.S.C. 102(b) as being anticipated by US Patent No. 6,223,305 of Simmons et al. referred hereinafter "Simmons".

In regards to claim 1, Simmons discloses a method comprising:

disabling selected functions of a computer system in response to an error (see column 12 lines 31-32);

issuing a set of diagnostic instructions to a processor (see column 12 lines 1-4);

In regards to claim 2, Simmons discloses:

incrementally enabling the selected functions until the error is reproduced. Simmons discloses events may be recreated in order to detect the error or malfunction (see column 12 lines 45-46);

In regards to claim 5, Simmons discloses:

setting a function disable register that is connected to a plurality of inhibit switches. Simmons disclose a switch command register to enable or disable the IMS (see column 12 line 27) indicating a function disable register. Simmons further discloses in response to a disable

signal, elements of the IMS are sequentially disabled one after another (see column 12 lines 31-32), indicating a plurality of inhibit switches.

In regards to claim 6, Simmons discloses an apparatus comprising:

means for disabling selected functions of a computer system in response to an error (see column 12 lines 31-32);

means for issuing a set of diagnostic instructions to a processor (see column 12 lines 1-4);

means for incrementally enabling the selected functions until the error is reproduced. Simmons discloses events may be recreated in order to detect the error or malfunction (see column 12 lines 45-46);

In regards to claim 9, Simmons discloses an apparatus comprising:

means for setting a function disable register that is connected to a plurality of inhibit switches. Simmons disclose a switch command register to enable or disable the IMS (see column 12 line 27) indicating a function disable register. Simmons further discloses in response to a disable signal, elements of the IMS are sequentially disabled one after another (see column 12 lines 31-32), indicating a plurality of inhibit switches.

In regards to claim 11, Simmons discloses an apparatus comprising:

detecting an error (see column 12 lines 17-21);

disabling selected functions of a computer system in response to the error (see column 12 lines 31-32);

issuing a set of diagnostic instructions to a processor (see column 12 lines 1-4);

incrementally enabling the selected functions until the error is reproduced. Simmons discloses events may be recreated in order to detect the error or malfunction (see column 12 lines 45-46);

In regards to claim 14, Simmons discloses an apparatus comprising:

setting a function disable register that is connected to a plurality of inhibit switches. Simmons disclose a switch command register to enable or disable the IMS (see column 12 line 27) indicating a function disable register. Simmons further discloses in response to a disable signal, elements of the IMS are sequentially disabled one after another (see column 12 lines 31-32), indicating a plurality of inhibit switches.

Claims 1, 3, and 4 are rejected under 35 U.S.C. 102(b) as being anticipated by US Patent No. 6,487,677 of Jantz et al. referred hereinafter "Jantz".

In regards to claim 1, Jantz discloses a method comprising:

disabling selected functions of a computer system in response to an error. Jantz discloses conveying information to a management device indicative of error, wherein in response of error conditions, executing diagnostic/recovery procedures (see column 4 lines 5-11). Jantz further discloses in response to success of the selected diagnostic/recovery procedures, normal operations are continued (see column 4 lines 61-65), implying normal operations are disabled until diagnostic/recovery procedures are successful, indicating disabling selected functions of a computer system in response to an error.

issuing a set of diagnostic instructions to a processor. Jantz discloses in response of error conditions, executing diagnostic/recovery procedures (see column 4 lines 5-11).

In regards to claim 3, Jantz discloses:

selecting the set based on a history of errors encountered by the computer system. Jantz discloses selecting the set based on historical trends in prior use of each recovery procedure (see column 5 lines 20-22)

In regards to claim 4, Jantz discloses:

selecting the set based on a class of the errors. Jantz discloses selecting a diagnostic/recovery procedures (see column 5 lines 18-20). In order to select a diagnostic/recovery procedure for an error from a plurality of diagnostic/recovery procedures, errors must be defined within different classes or types.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 16, 19, and 20 are rejected under 35 U.S.C. **103(a)** as being unpatentable over US Patent No. 6,145,102 of Klein et al. referred hereinafter "Klein" in view of US Patent No. 6,125,465 of McNamara et al. referred herein "McNamara" .

In regards to claim 16, Klein discloses a computer system comprising:

a processor (see figure 1 item 107 and column 1 lines 40-43);

enabling and disabling the processor (see column 1 lines 40-43);

However, Klein fails to explicitly disclose:

a plurality of inhibit switches to selectively enable and disable a corresponding plurality of functions of the processor;

a function disable register to control the plurality of inhibit switches;

a shift unit to incrementally change the contents of the function disable register

McNamara further discloses

a plurality of inhibit switches to selectively enable and disable a corresponding plurality of functions of the processor. McNamara discloses clock control macros which can stop the system clock to the functional unit (see figure 1 items 15,16,17,18 and column 2 lines 33-44);

a function disable register to control the plurality of inhibit switches. McNamara discloses a GPTR, which when a bit is set, stops the system clock to the functional unit corresponding to the bit (see figure 1 item 10 and column 2 lines 40-44);

a shift unit to incrementally change the contents of the function disable register. McNamara discloses setting the binary values to "1" (see column 40-44).

It would have been obvious to one of ordinary skill in the art at the time of the invention was made to combine the teachings of Klein and McNamara to have a plurality of inhibit switches to selectively enable and disable a corresponding plurality of functions of the processor, a function disable register to control the plurality of inhibit switches, and a shift unit to incrementally change the contents of the function disable register. A person of ordinary skill in the art would have been motivated to combine the teaching because Klein is concerned with enabling and disabling computer system components such as the processor when there is an error (see column 1 lines 40-43) and having a plurality of inhibit switches to selectively enable and disable a corresponding plurality of functions of the processor, a function disable register to

control the plurality of inhibit switches, and a shift unit to incrementally change the contents of the function disable register, as per teachings of McNamara (see figure 1 and column 2 lines 33-44), provides a suitable means to enable an disable computer system components such as the processor when there is an error.

In regards to claim 19, Klein in view of McNamara discloses the claim limitations as disclosed above. Klein further discloses a memory connected to the processor and disabling functions of the memory (see column 1 lines 40-43). As McNamara discloses the means to disable a component using inhibit switches to selectively enable and disable a function of a component, wherein the function disable register is to control the inhibit switches (see figure 1 and column 2 lines 33-44), using McNamara's means to disable a component to disable the memory as disclosed in Klein would further disclose a memory connected to the processor and an additional inhibit switch to selectively enable and disable a function of the memory, wherein the function disable register is to control the inhibit switches.

In regards to claim 20, Klein in view of McNamara discloses the claim limitations as disclosed above. Klein further discloses a bus connected to the processor and disabling functions of the bus (see column 1 lines 40-43). As McNamara discloses the means to disable a component using inhibit switches to selectively enable and disable a function of a component, wherein the function disable register is to control the inhibit switches (see figure 1 and column 2 lines 33-44), using McNamara's means to disable a component to disable the bus as disclosed in Klein would further disclose a bus connected to the processor and an additional inhibit switch to selectively enable and disable a function of the bus, wherein the function disable register is to control the inhibit switches.

Allowable Subject Matter

Claims 7, 8, 17, and 18 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claim 12 and 13 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 101 set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

Claim 10 would be allowable if rewritten to overcome the Claim Objection set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

Claim 15 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 101 and Claim Objection set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

See Form PTO-892.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Emerson C. Puente whose telephone number is (571) 272-3652. The examiner can normally be reached on 8-5 M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert W. Beausoliel can be reached on (571) 272-3645. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Emerson Puente

Emerson Puente
Examiner
AU 2113